EE/CprE/SE 4920 STATUS REPORT 4

28FEB2025 – 13MAR2025
Group number: sdmay25-04
Project title: Wireless Mesh Network for Pesticide Spray Monitoring and Mapping

Client: Claussen Lab- Iowa State University

Advisor: Nathan Niehart

Team Members/Role:
Software Team

- **Ashley Falcon:** IDEs and Microcontrollers, Group Communicator
- **Drew Scheidler:** Mesh Networking; Note Taker
- **Henry Hingst:** Mesh Networking; Group Leader

Hardware Team

- **Hector Perez Prieto:** Microcontroller; Circuit Design and Testing
- **Yok Quan Ong:** Circuit Design and testing; Microcontroller
- **Wesley Smith:** Circuit Design/Simulation; Microcontrollers; Note Taker

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Period Summary

- Hardware Team Summary:

The hardware team finalized the PCB design and the BOM and moved forward with ordering everything from ETG. In order to finalize the PCB layout we needed to change the setting of the layout to a wider trace ensuring we could fit all the components. We also made a lot of final decisions for the parts we would be including in our final design. Last status report, we were looking into a way to solve our issue regarding having too few pins on the microcontroller and we decided to share the external ADC's clock pins.

- Software Team Summary:

The software team this week met and aligned our milestones for completing the remainder of the project. We made the decision to not use the Espressif wifi mesh system for our communication and instead use LoRa packet transmitters instead. We created pseudocode and block diagrams to visualize better what the conglomeration of our code would look like and account for program flow. We have considered the user and the steps the code will walk through to record, process, and transmit data. Individually, we continued to work on our specific segments, such as testing transmission on LORA boards and creating a new iteration of the ADC driver code to account for our use of an external one.

Past Period Accomplishments

Our hardware and software teams met milestones and accomplishments over the past two weeks. Here are our individual contributions:

- Ashley Falcon:
    - Finished the first iteration of the ADC driver code
        - This will allow our microcontroller to draw data from the external ADC
        - Initially used SPI
            - Seemed to overcomplicate the code
            - It wasn't as reliable or clean as simply reading the pin as high or low and altering the bits accordingly
        - Now am using a clock toggle method
            - Set clock high → read data pin state → add to binary code → set clock low
            - Created conversion helper method to transform raw ADC data into voltage data
    - Met with the SW team
        - Established milestones and responsibilities
        - This will allow our team to implement designs in a more cohesive manner
        - Determine our next steps and timelines

- Drew Scheidler:
    - Set up circuit and code to test LoRa range
        - Programmed code to count sent packets
        - Sender sends packets with a count
        - Receiver code displays received packets
        - Receiver code notifies when a packet was missed based on received count being out of order
        - Set up LEDs
            - Green LED blinks when a packet is received
            - Red LED blinks when code detects packet miss
    - Ordered parts required to hook LoRa module to an actual antenna
    - Sorting out high level organization of code
        - Helped design pseudocode for base and measurement nodes
        - Helping to design block diagram for base and measurement nodes code

- Henry Hingst:
    - Began familiarizing myself with the LoRa modules and how to use them
        - Our order for them didn't arrive until the end of this report period so I wasn't able to physically test or use them
    - Began designing our first prototype
        - Created a block diagram of what each node type is going to do
        - Created pseudocode from the block diagram as a basis for the software of our first prototype
        - Specified packet formats for each type of packet that will be sent on the network
        - Specified what steps our users will need to take in order to set up and use our first prototype

- Hector Perez Prieto:
    - Assisted in ensuring one voltage reference generator could not drive three sensor circuits
        - Led to decision of having one voltage reference generator per sensor
    - Found best placements for decoupling capacitors on the PCB design to ensure stable voltages with no fluctuations
    - Updated BOM with new components and finalized

- Yok Quan Ong:
    - PCB Layout
        - Resize the PCB, make it larger
        - Select component from Digikey
    - Update and finalized BOM

- Wesley Smith:
    - Redid simulations and math
        - Make sure the Vrefs can drive the circuit
        - Simulate worst case
        - Calculate circuit run time
    - Updated and finalized BOM for the creation of three boards with necessary parts
    - Began work on a testing plan

NAME	Individual Contributions	Hours this Period	Cumulative Hours
Ashley Falcon	Finished and reviewed ADC driver code	**12**	**43**
Drew Scheidler	Setting up LoRa range testing, High-level code organization	**15**	**57**
Henry Hingst	Software Block Diagram and Pseudocode	**20**	**40**
Hector Perez Prieto	Component placement, BOM finalization	**13**	**43**
Yok Quan Ong	PCB Layout, BOM updated	**15**	**48**
Wesley Smith	Simulation, Updated BOM	**12**	**42**

Plans for the upcoming period

- **Hardware Team**
    - Create a plan for the upcoming testing for the testing of the parts and PCBs ordered this week
    - Solder the PCBs

- **Software Team**
    - Create a second iteration of ADC driver code by implementing interrupts rather than polling
        - Edit to include error flags and account for multiple resolution switching circuits
    - Collaborate further with Drew and Henry to create more thorough timelines and milestones
    - Begin cohesively bringing our individual codes together
        - Ideally, by the next period, we will have a PCB where we can begin testing
    - Collaborate with the HW team to ensure their requirements are met, and we are not missing anything critical
    - Test LoRa range
    - Find out if LoRa board buffers
    - Case testing SD code specifics
    - Finish block diagram
    - Delegate code segments

Summary of Weekly Advisor Meetings

- Week 6 (Mar 4th)
    - **Hardware:**
        - Add decoupling capacitor for the sensor circuit
        - We don’t need an external reset button
        - Research if we need a heat sink for the project
        - Add ground test point around the board
        - Resize and re-layout the board
        - Get the LoRa footprint figure out
    - **Software:**
        - Research implementation of interrupts in the ADC code
        - Change from SPI communication to manually toggling in the ADC
        - Iron-out data flow timing
            - All ADCs will have the same clock
            - Read ADC one at a time:
                - Enable, Read, Disable, Repeat
            - Full system timing once code is compiled
        - Range testing should be conducted
        - Brainstorm approach to sensor IDs

- Week 7 (Mar 11th)
    - **Hardware:**
        - Get the PCB ordered
        - Send the BOM to ETG
        - Get the board solder once we received it
        - Make a test plan
    - **Software:**
        - Make a block diagram of signal flow and overall architecture
            - Block diagram and pseudocode
        - Implement interrupts in ADC code
            - Also, begin checking status bits to determine if errors occur
            - Erroneous conversions will be discarded rather than recovered
                - Record overall number of conversions to see how much data is lost if any
        - Determine if LORA has interrupt flags or buffers
        - Finalize milestones and tasks and send to advisor